



SSC8333GS1

Dual P-Channel Enhancement Mode MOSFET

➤ Features

VDS	VGS	RDS(on) Typ.	ID
-30V	±20V	61mR@-10V	-4.5A
		77mR@-4V5	

➤ Description

This device is produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wide range of given voltage ratings(4.5V~25V) such as load switch and battery protection.

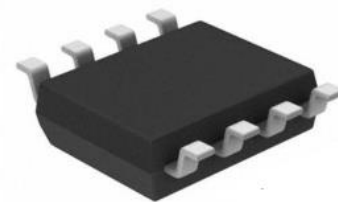
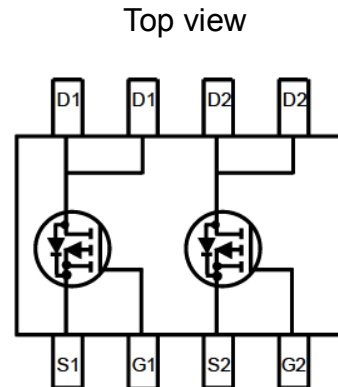
➤ Applications

- TFT panel power switch
- High Side DC/DC Converter
- High Side Driver for Brushless DC motor
- Portable DVD, DPF

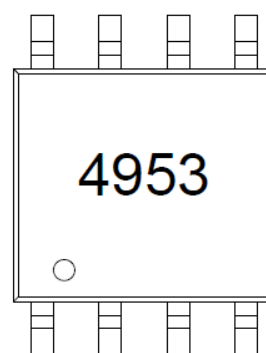
➤ Ordering Information

Device	Package	Shipping
SSC8333GS1	SOP-8	2500/Reel

➤ Pin configuration



Bottom View



Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-30	V
V_{GSS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current ^a	-4.5	A
I_{DM}	Pulsed Drain Current ^b	-20	A
P_D	Power Dissipation ^c	2	W
P_{DSM}	Power Dissipation ^a	1.2	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		110	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		70	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^{\circ}\text{C}$.The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_J(\text{MAX})=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

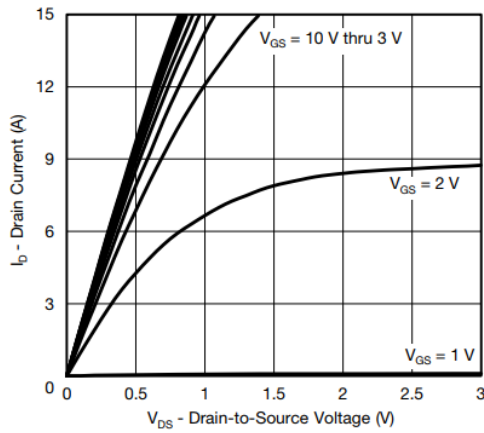


➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

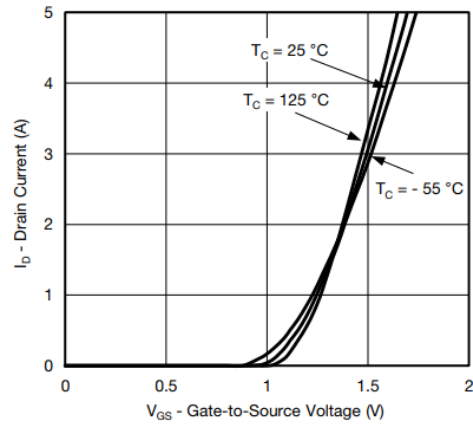
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.4	-3	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-10V, I_D=-6A$		61	70	mR
		$V_{GS}=-4.5V, I_D=-4A$		77	85	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=-1A$		-0.8	-1.5	V
G_{FS}	Transconductance	$V_{DS}=-5V, I_D=3.6A$		5		S
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		550		pF
C_{oss}	Output Capacitance			60		
C_{rss}	Reverse Transfer Capacitance			50		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-10V,$ $V_{DS}=-15V, R_G=3R, R_L=2.5R$		9		ns
T_r	Rise time			6		
$T_{D(OFF)}$	Turn-off delay time			28		
T_f	Fall time			4		
Q_g	Total Gate charge	$V_{GS}=-4.5V, V_{DS}=-15V,$ $I_D=-3A$		13		nC
Q_{gs}	Gate to Source charge			1.6		
Q_{gd}	Gate to Drain charge			1.5		



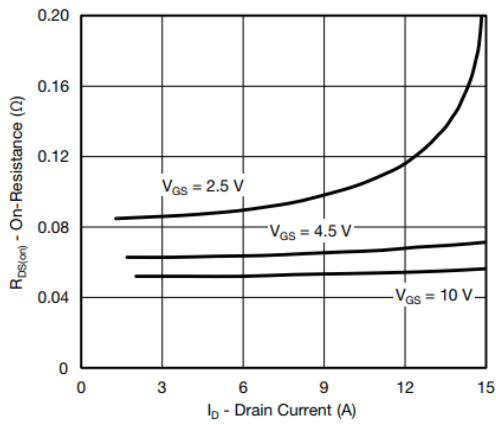
➤ **Typical Characteristics** ($T_A = 25^\circ\text{C}$ unless otherwise noted)



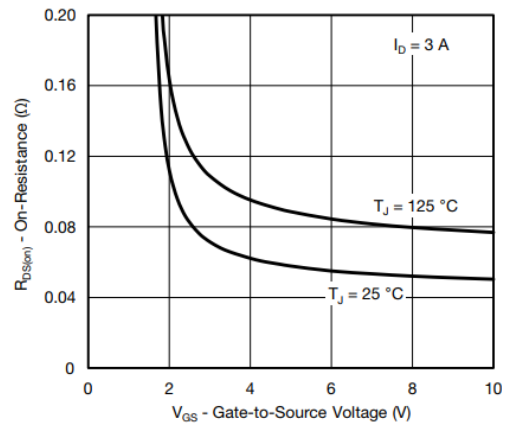
Output Characteristics



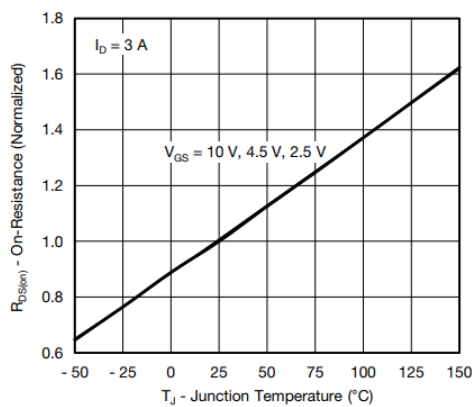
Transfer Characteristics



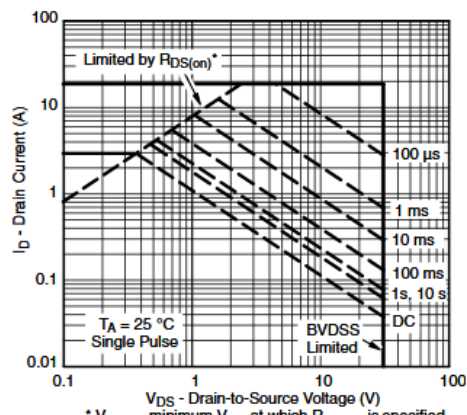
On-Resistance vs. Drain Current and Gate Voltage



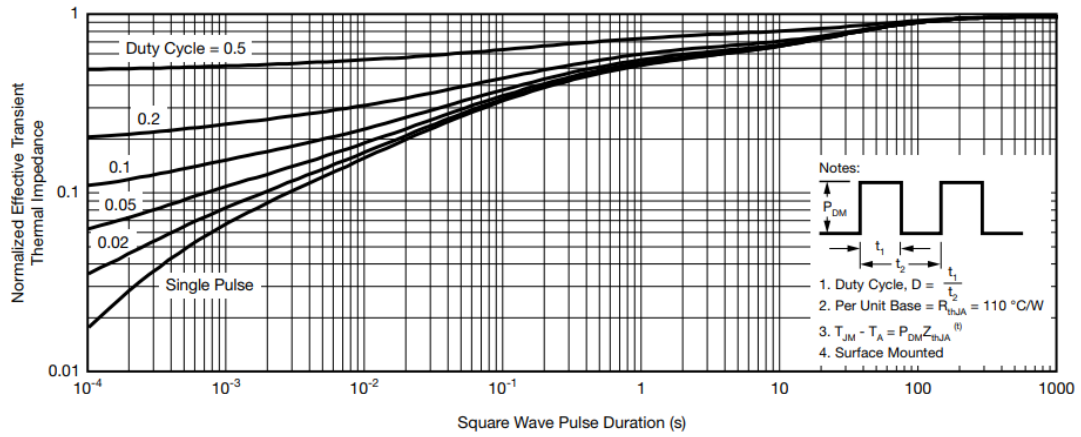
On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature



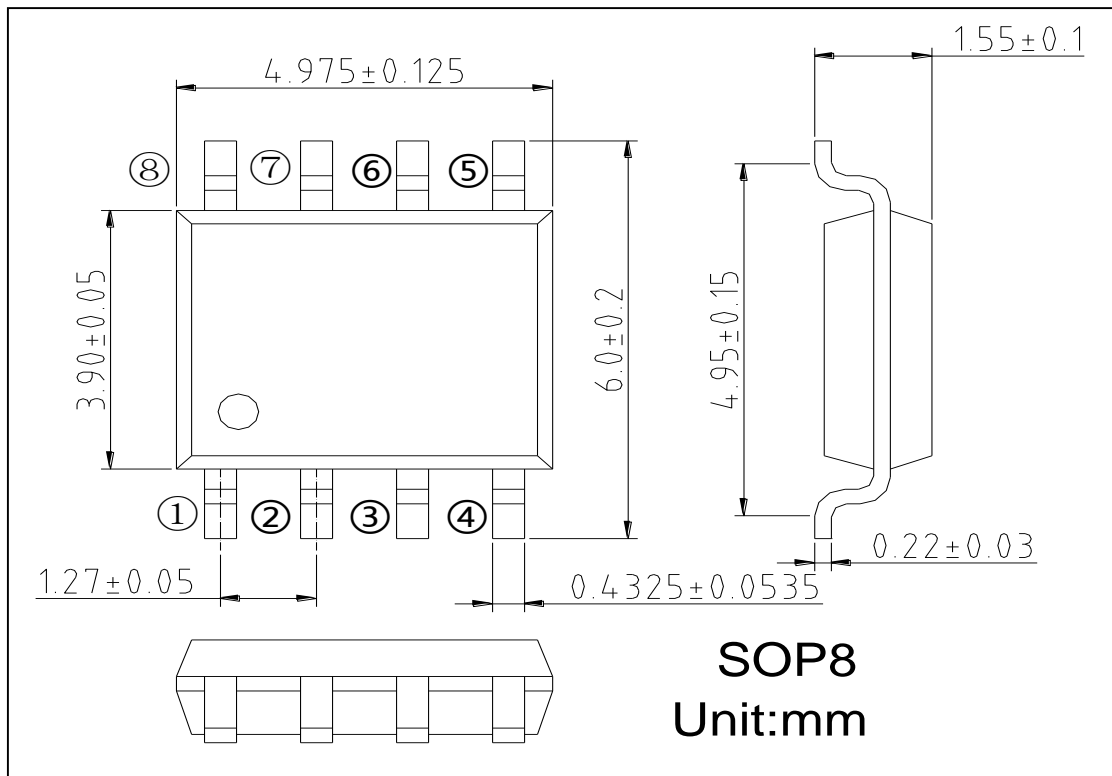
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



➤ Package Information



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